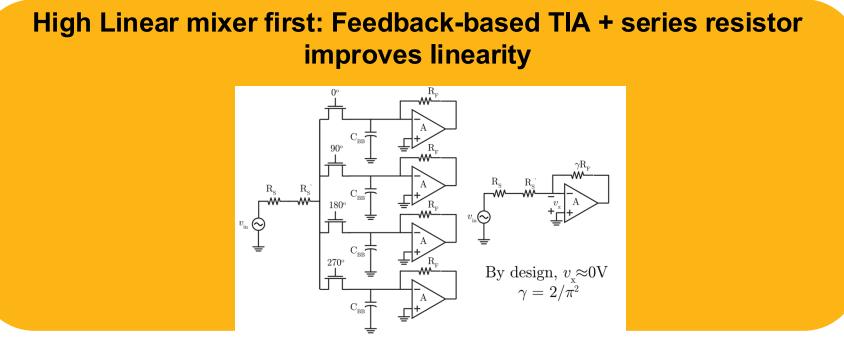
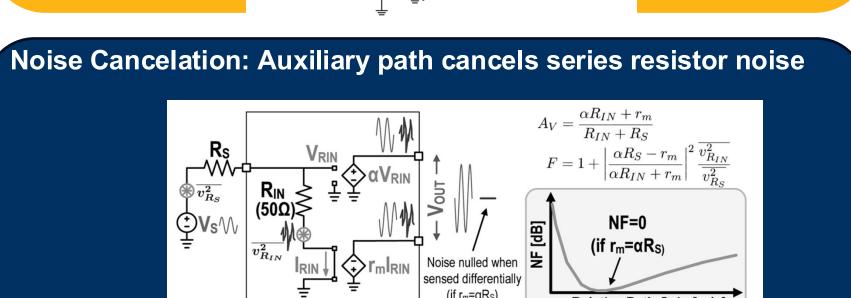
Wideband Ultra Linear Transceiver Circuits (WULT-C) for New Spectrum

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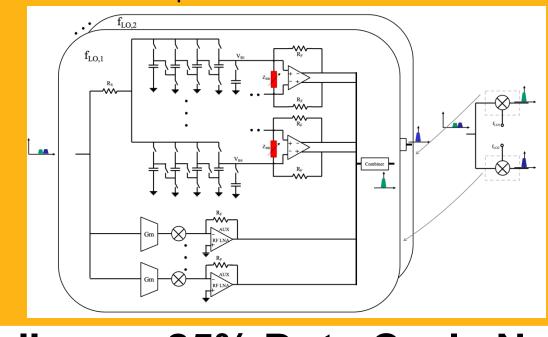
Wideband Programmable High Linear Receiver

- ☐ Wireless data rates continue to grow, requiring much wider bandwidths.
- ☐ FR3 (7–24 GHz) offers a good trade-off between bandwidth and coverage.
- ☐ Splitting the spectrum into narrow bands limits flexibility and performance.
- ☐ Carrier aggregation requires a wideband RX capable of receiving multiple channels simultaneously.
- ☐ The RX must achieve high linearity, low noise figure (NF), good input matching, and sharp filtering selectivity.
- ☐ Previous Art:

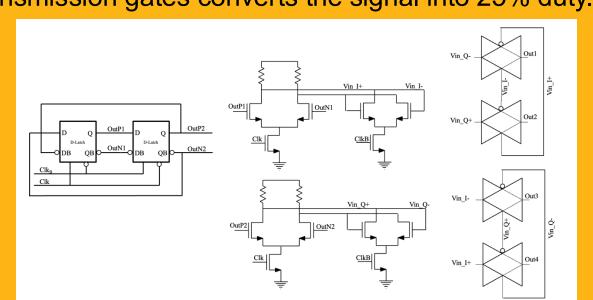




- ☐ Possible Solutions:
 - Mixer-first per-channel.
 - Zero-IF (ZIF) conversion for each carrier.
 - ➤ Mixer should also see high order Z_{BB}
 - Passes are separated.



- ☐ Challenge: 25% Duty Cycle Non-Overlapping Signals
 - Commonly generated using digital techniques.
 - D-latches generate in-phase and quadrature signals.
 - Then active inverters make the signals to the levels.
- Transmission gates converts the signal into 25% duty.



Signal period is 25ps for 10GHz input clock.

Passive mixer with gain stack replaces LNA.

High rejection N-path filter in second stage.

Series resistor matching + noise cancellation.

Parallel loading should be cancelled out by serializing.

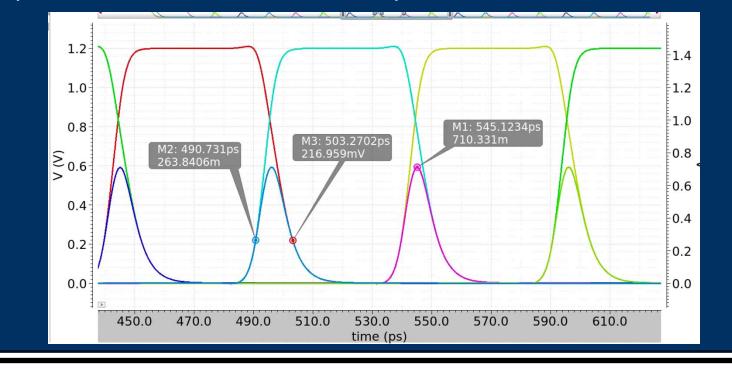
- Simulation includes the parasitics.
- > Overlap of the waveforms is around 13ps when transistors are around Vth.

High Order N-path Filter: sharp out-of-band rejection (-40 to

-80 dB/dec)

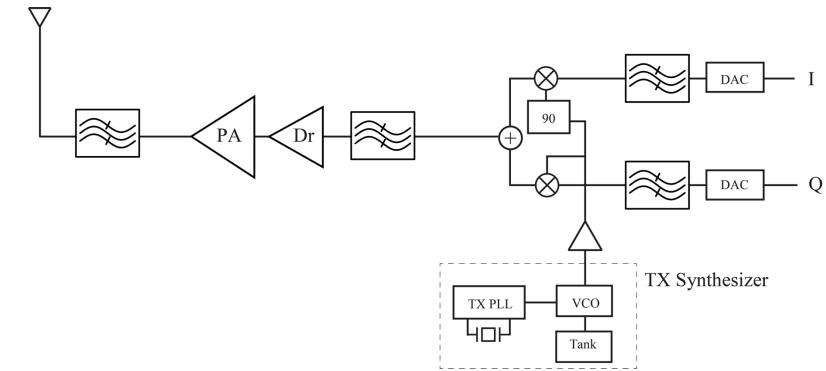
Passive Voltage Gain & Harmonic Cancellation: Passive

stacking + charge sharing for harmonic suppression



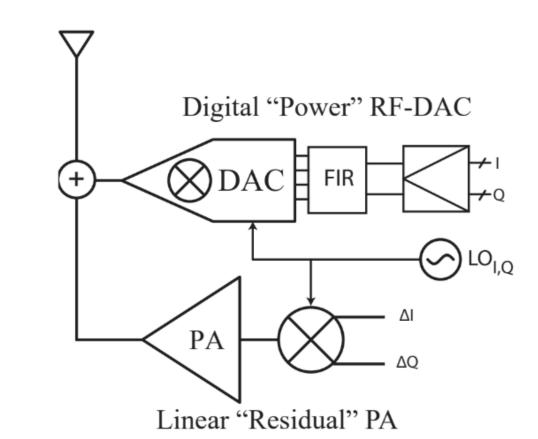
Hybrid Digital Power Amplifier

□ Conventional Transmitters:



- Traditional Tx requires linear PA but benefits from high resolution IQ baseband DAC filter to minimize harmonics and other out-of-band emissions.
- RF-DAC is simpler and can scale with CMOS due to switching nature of core PA. Inherently "linear" due to DAC operation.

☐ Proposed Hybrid Digital PA:



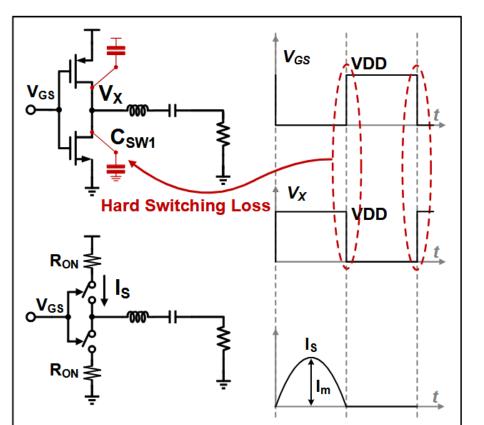
- ❖ RF-DAC for high and efficient power and highly linear
- Second PA to reduce quantization noise:
- Improved dynamic range / reduced quantization noise floor and OOB emissions
- Higher bits of resolution

❖ Inverse Class-D

Zero voltage switching (ZVS)

Digital PA Architectures:

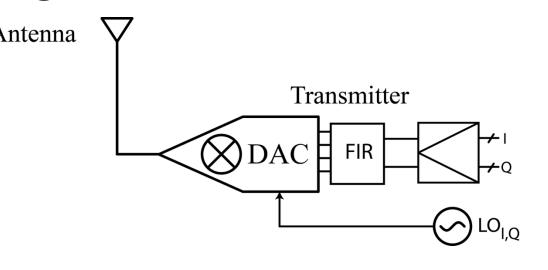
❖ Class-D



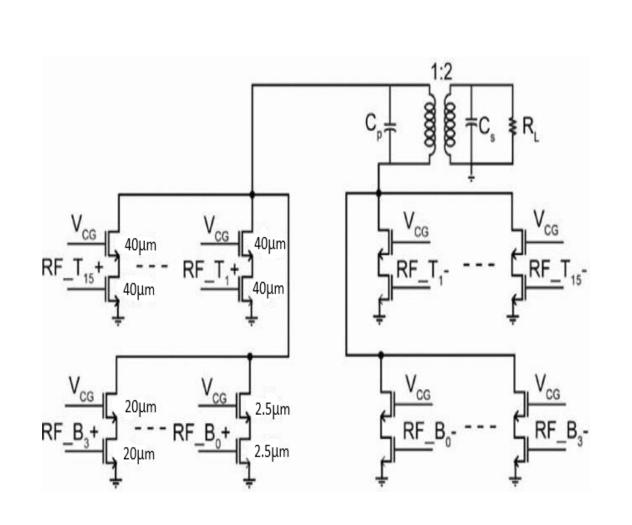
- Hard switching loss at high freq
- ☐ Performance comparison between Class-D and Inverse Class-D PA at 10GHz in CMOS 28nm technology:

	Pout (dBm)	Drain Efficiency (%)	VDD
Class-D	12.4	63.8	2
Inverse Class-I	12	72	0.8

□ Digital PA Transmitters:



- ☐ Polar "Digital" PA:
- ✓ High linearity
- ✓ High peak efficiency
- ✓ Real-time controllability and reconfigurability
- X Limited ENOB for digital mm-wave PA



Inverse Class-D PA architecture. B0-B3 are binary weighted LSBs, T1-T15 are thermometer coded MSBs.

- **VDD=1.5 V**
- Pout=25.6 dBm
- Drain Efficiency=76.5 %

□ Waveforms:

